REMARKS

Claims 1, 3-10, and 29-31 stand "rejected under 35 U.S.C. 103(a) as being unpatentable over" Applicants' Specification (AAPA) in view of Matsuura et al. (U.S. Patent No. 5,132,774). Claim 32 stands "rejected under 35 U.S.C. 103(a) as being unpatentable over" AAPA in view of Matsuki et al. (U.S. Patent No. 5,960,252). Claims 1 and 32 have been amended to include the features of claim 3. Claim 33 is newly added and includes the features of claim 1 (prior to the present amendment) and claim 5. Claim 34 is newly added and includes the features of claim 32 (prior to the present amendment) and claim 5. Claims 3 and 5 have been cancelled. No new matter has been added.

Reconsideration and allowance of claims 1, 4, 6-10 and 29-34 are respectfully requested.

Applicants' Specification (i.e., Figures 10A-10E and supporting text) discloses a semiconductor device including a second interlayer insulating film formed of a plasma TEOS film having compressive stress. The compressive stress prevents the polarization of a dielectric material that forms a dielectric film that is included in the semiconductor device (See originally filed application at page 5, lines 4-8).

Matsuura teaches a method of forming an interlayer insulating film that insulates first and second layers of conductor patterns in a semiconductor device (See Matsuura, Abstract).

Matsuki discloses a method of manufacturing a nonvolatile semiconductor memory device including a ferroelectric capacitor (See Matsuki, Abstract). In the present Office Action, Matsuki is relied upon to teach that TEOS films may be subjected to tensile stress (See Matsuki, column 6, lines 54-59) (See Office Action, page 3).

Applicants' invention, as recited by claim 1, as amended, includes features that are neither disclosed nor suggested by the art of record, including:

> ... a capacitor ... a first interlayer insulating film ... to directly cover the capacitor...a first interconnect ... provided on the first interlayer insulating film and electrically connected to the

> integrated circuit and the capacitor ... a second interlayer insulating film having a tensile stress ... to directly cover the first interconnect and the first interlayer insulating film...a second interconnect ... provided on the second interlayer insulating film and electrically connected to the first interconnect ... the second interconnect is provided on the second interlayer insulating film ... to cover at least a part of the capacitor...

This means that the semiconductor device recited in claim 1 includes a capacitor that is directly covered by a first interlayer insulating film. A first interconnect is electrically connected to the capacitor through a hole in the first film. A second interlayer insulating film having tensile stress directly covers the first interconnect and the first film. A second interconnect, provided on the second film, is electrically connected to the first interconnect through a hole in the second film. The second interconnect covers at least a part of the capacitor.

In rejecting claims 1, 3-10, and 29-31, the present Office Action refers to the Office Action dated April 9, 2002 to provide the details of the rejection. The Office Action dated April 9, 2002, refers to Figures 1E and 6A-B of Matsurra in the rejection of claim 1.

More specifically, the Office Action dated April 9, 2002 indicates that Figure 1E of Matsuura discloses a second film 14 having tensile stress and directly covers first interconnect 12 and first film 20 (See page 3 of Office Action dated April 9, 2002). Of initial interest is that the embodiment illustrated in Figure 1E does not illustrate a capacitor but rather illustrates a substrate 11 including transistors (See Matsuura, column 4, lines 42-44). As such, first film 20 clearly does not directly cover a capacitor, as recited in claim 1. Further, first interconnect 12 is not electrically connected to a capacitor through a hole in first film 20.

Additionally, Figure 1E illustrates a portion of conductive layer 12 that is connected to substrate 11 through a hole in film 20. Apparently, it is this portion of conductive layer 12 that is analogous to the first interconnect of claim 1, because it is the only portion of conductive layer 12 that is connected to a lower structure through a hole in film 20; however, second interconnect 18 in Figure 1E is not

electrically connected to this portion of conductive layer 12, and as such, another limitation of claim 1 is not disclosed in Figure 1E. Further still, second interconnect 18 is not provided on second film 14 so as to at least partially cover a capacitor (as in claim 1), because, as indicated above, Figure 1E does not even disclose a capacitor.

As such, the structure of Matsuura, as disclosed in Figure 1E, is very different from the structure recited in claim 1.

Turning now to Figures 6A-6B of Matsuura, a capacitor (27-29) is disclosed. The Office Action dated April 9, 2002 indicates that Figures 6A-6B illustrate second film 35 having tensile stress directly over first interconnect 32/34 (i.e., bit line 32 and first layer wire 34) and first film 33; however, second film 35 does not directly cover first bit line 32, as required by claim 1. Further, second interconnect 36 is not shown in Figure 6A as being electrically connected to bit line 32 (they are separated by insulating films 33 and 35) or first layer wire 34 (they are separated by insulating film 35), as required by claim 1. While Figure 6B does illustrate second interconnect 36 connected to first layer wire 34, second interconnect 36 does not cover at least a portion of a capacitor in Figure 6B, as required by claim 1.

As such, the structure of Matsuura, as disclosed in Figures 6A-6B, is very different from the structure recited in claim 1.

Matsuura and AAPA do not make up for the deficiencies of Matsuura with respect to claim 1. It is because Applicants include the above-recited features in claim 1 that the following advantages are achieved. A semiconductor device is provided with reduced stress on the capacitor, thereby improving the operational characteristics of the capacitor.

Therefore, claim 1 is patentable over AAPA, Matsuki, Matsuura, and any combination thereof. Claims 4, 6-10, and 29 include all of the features of independent claim 1 from which they depend, either directly or indirectly. Accordingly, claims 4, 6-10, and 29 are also patentable over AAPA, Matsuki, and Matsuura for the reasons set forth above. Claims 30-34, while not identical to claim 1, include features similar to those recited above with respect to claim 1. As such,

claims 30-34 are also patentable over AAPA, Matsuki, and Matsuura for the reasons set forth above.

Applicants' invention, as recited by claim 33, includes an additional feature that is neither disclosed nor suggested by the art of record, namely:

> ... a hydrogen supplying layer provided between the first interconnect and the second interlayer insulating film excluding an area in which the capacitor is provided.

This means that the semiconductor device recited in claim 33 includes a hydrogen supplying layer between the first interconnect and the second interlayer insulating film. The hydrogen supplying layer is not provided in an area in which the capacitor is provided.

This feature of claim 33 was previously included in claim 5 (before being cancelled claim 5 was dependent upon claim 1). In rejecting claim 5, the present Office Action refers to the Office Action dated April 9, 2002 to provide the details of the rejection. The Office Action dated April 9, 2002, refers to Figures 1E and 5A-B of Matsurra in the rejection of claim 5. More specifically, the Office Action indicates that the layers 13 and 16 in Matsuura could include silicon nitride (See Matsuura, Figure 5B, column 7, lines 1-10). Figure 5B of Matsuura teaches to form layer 13 directly on a first layer conductor 12; however, Figure 5B does not teach a capacitor at all. Figure 6B of Matsuura does illustrate a capacitor (27-29); however, Figure 5B and Figure 6B of Matsuura illustrate very different applications (See Matsuura, column 4, lines 11-14). As such, layers 13 and 16 of Figures 5A-5B could not be provided in an area of a semiconductor device away from a capacitor because no capacitor is illustrated in Figures 5A-5B.

Further, the hydrogen supplying layer recited in claim 33 excludes the area where the capacitor is formed; however, Matsuura teaches forming silicon nitride films 13 and 16 across the entire surface of Figures 5A-5B; no area or circuit element (e.g., a capacitor) is excluded. As such, claim 33 is clearly distinguished from Matsuura.

AAPA and Matsuki do not make up for the deficiencies of Matsuura with respect to claim 33. Matsuki does teach a first insulating film 20 formed by sputtering silicon oxide or silicon nitride; however, since the silicon nitride in Matsuki

is formed by sputtering, it is completely unclear whether it would contain enough hydrogen to act as a hydrogen supplying layer or not. Matsuki does not mention a hydrogen supplying effect at all, and, in fact, Matsuki teaches to reduce the amount of hydrogen in the layers in order to reduce the aforementioned water problem (See Matsuki, column 2, lines 21-30). Therefore Matsuki teaches away from providing a hydrogen supplying layer as in claim 33.

Accordingly, claim 33 is patenable over the AAPA, Matsuura, and Matsuki for this additional reason. Claim 34, while not identical to claim 33, includes features similar to those recited above with respect to claim 33. Accordingly, claim 34 is also patentable over AAPA, Matsuura, and Matsuki for this additional reason.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully Submitted,

Andrew L. Ney

Andrew L Ney, Reg. No. 20,300
Attorney for Applicants

ALN/CS/ap/dm

Enclosures:
Version with markings to show changes made
Dated: February 11, 2003
P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700
The Assistant Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. 18-0350 of any fees associated with this communication.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (703-746-3891) on the date shown below.

February 11, 2003
Danielle Murphy

VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS:

1. (As Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode, said dielectric film being formed from either a dielectric material having a high dielectric constant or a ferroelectric material;

a first interlayer insulating film provided so as to directly cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film;

a second interlayer insulating film having a tensile stress provided so as to directly cover the first interconnect and the first interlayer insulating film;

a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film; and

a passivation layer provided so as to cover the second interconnect, wherein the second interconnect is provided on the second interlayer insulating film so as to cover at least a part of the capacitor.

32. (As Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode;

a first interlayer insulating film provided so as to directly cover the capacitor, the first interlayer insulating film having a tensile stress;

a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film;

a second interlayer insulating film having a tensile stress provided so as to directly cover the first interconnect and the first interlayer insulating film;

a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film; and

a passivation layer provided so as to cover the second interconnect, wherein the second interconnect is provided on the second interlayer insulating film so as to cover at least a part of the capacitor.

Claims 3 and 5 are cancelled.

Claims 33 and 34 have been newly added.